Claims

What is claimed is:

1. A method of elevating a potential of a transimpedance amplifier input port comprising the steps of:

providing a long tail pair of transistors including a first transistor having a base terminal coupled with the transimpedance amplifier input port and a second transistor having a base terminal for receiving a first bias voltage, the emitter terminals of both transistors coupled to an AC ground terminal;

providing the first bias voltage to the base terminal of the second transistor; and,

shifting a DC saturation voltage of the first transistor by providing an approximately equal DC voltage to the transimpedance amplifier input port as the DC voltage provided to the base terminal of the second transistor.

2. A method according to claim 1, wherein the step of shifting the saturation voltage comprises the steps of:

providing a first current source for providing a first current to the emitter terminals of the long tail pair of transistors; and,

biasing the emitter terminals at a first predetermined bias voltage using the first current.

3. A method according to claim 1, wherein the step of shifting the saturation voltage comprises the steps of:

providing an emitter follower circuit connected to one of the emitter and collector terminals of one of the transistors forming the long tail pair;

providing a second current source for providing a second current the emitter follower circuit in dependence upon a bias signal received on a bias port thereof.

4. A method according to claim 1, comprising the steps of:

providing a first supply voltage input port with a potential of approximately 3.3V; and,

providing a second supply voltage input port with a ground potential, where a bias voltage of the transimpedance amplifier input port is approximately 1.5V above a potential of the AC ground terminal.

5. A method according to claim 1, wherein a saturation voltage of the first transistor is greater than 0.8V.

6. A method of increasing a reverse bias voltage for a PIN diode having an anode terminal coupled to an transimpedance amplifier input port of a transimpedance amplifier and having a cathode terminal coupled to a positive supply voltage input port having a first DC potential comprising the steps of:

providing a long tail pair of transistors including a first transistor having a base terminal coupled the transimpedance amplifier input port and a second transistor;

providing a DC bias voltage having a value equal to the first DC potential minus a second DC potential to the base terminal of the second transistor resulting in the first transistor having a base terminal DC potential approximately equal to that of the first DC potential minus the second DC potential; and,

reverse biasing the PIN diode with the second DC potential.

7. A method according to claim 6, wherein the first DC potential minus the second DC potential has a resultant potential that is greater than 0.7V..

8. A method according to claim 6, wherein the first DC potential is approximately 3.3V and the first DC potential minus the second DC potential has a resultant potential of approximately 1.5V.

9. An elevated front-end transimpedance amplifier comprising:

a first supply voltage input port for receiving a first DC potential;

a second supply voltage input port for receiving a second DC potential that is lower than that of the first DC potential;

an input stage comprising a long tail pair of transistors comprising a first transistor having a base terminal coupled with a transimpedance amplifier input port and a second transistor having a base terminal for receiving a first DC bias voltage, one of the emitter and collector terminals of first and second transistors coupled together and the other of the terminals for receiving at least a portion of the first DC potential;

an input stage bias port coupled to the base terminal of the second transistor for receiving an input stage DC bias voltage; and,

a first current source for shifting a DC saturation voltage of the first transistor by providing an approximately equal DC voltage on the transimpedance amplifier input port as the first DC bias voltage provided to the base terminal of the second transistor.

10. An elevated front-end transimpedance amplifier according to claim 9, wherein the first current source is for providing a first current from a first current output port to one of the emitter and collector terminals of first and second transistors forming the long tail pair.

11. An elevated front-end transimpedance amplifier according to claim 10, wherein the first transistor has one of the emitter terminal and collector terminal coupled to an input stage output port and the other terminal is coupled to the first current source for receiving the first current therefrom.

12. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 9, comprising a diode, where one of the emitter terminal and collector terminals of the second transistor are connected thru the diode to the first supply voltage input port.

13. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 10, comprising an output stage comprising a third transistor, the third transistor having a base terminal coupled to the input stage output port and one of the emitter

terminal and the collector terminal coupled to a transimpedance amplifier output port and the other terminal coupled to the first supply voltage input port.

14. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 13, comprising:

a second current source having a second current source output port; and,

an output resistor, the output resistor coupled in series between the second current source output port and the EFTIA output port.

15. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 10, comprising a feedback resistor, the feedback resistor connected between the second current source output port and the transimpedance amplifier input port for propagating the feedback signal to the transimpedance amplifier input port for determining a gain of the EFTIA.

16. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 13, comprising a resistor network, the resistor network coupled in series between the first supply voltage input port and the input stage output port for determining an output signal level provided from the input stage output port to the output stage input port.

17. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 16, comprising a third capacitor disposed in parallel with a portion of the resistor network for providing zero pole compensation to the EFTIA, when the EFTIA is in use.

18. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 9, comprising a first capacitor disposed between the second supply voltage input port and the second current source output port for providing a low impedance path to the second supply voltage input port for high frequency input signals received from the long tail pair of transistors.

19. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 9, comprising a second capacitor disposed between one of emitter and collector terminals of the second transistor and the second supply voltage input port, the second capacitor for limiting noise in the EFTIA, when the EFTIA is in use.

20. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 9, comprising a fourth capacitor disposed between the input stage bias port and the second supply voltage input port. {Steve} O.K. this is C4.

21. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 10, comprising a fifth capacitor in parallel with a portion of the second current source for limiting noise in the EFTIA, when in use.

22. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 10, wherein the first current source comprises a MOS transistor.

23. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 10, wherein the second current source comprises a transistor in series with a resistor.

24. An elevated front-end transimpedance amplifier circuit (EFTIA) according to claim 9, wherein the EFTIA is fully integrated on an integrated semiconductor substrate using a BiCMOS process.